IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Hiroshi SHIMIZU

Serial Number: 10/629,809

Filed: July 30, 2003

Allowed: January 13, 2005

Confirmation Number: 7790

Group Art Unit: 2818

Examiner: Gene Nghia Auduong

For: SEMICONDUCTOR MEMORY HAVING HIERARCHICAL BIT LINE STRUCTURE

AMENDMENT AFTER ALLOWANCE UNDER RULE 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Date: March 11, 2005

Sir:

Prior to issuance of the above-identified application, please amend the application as follows: